What Is Claimed Is:

1. A method, comprising:

receiving a new store into an instruction window;

storing a previous store into a second level circuit, wherein said second level circuit includes at least one block associated with a checkpoint; and

inserting a subsequent store into said instruction window.

2. The method of claim 1, said receiving a new store further compromising:

allocating an entry at a tail of a first level store queue;

monitoring said first level store queue, wherein said monitoring includes determining when said first level store queue is full;

determining a previous store from a head of said first level store queue;

determining a subsequent store, wherein said subsequent store needs to be inserted into said instruction window; and

removing said previous store from said head of said first level store queue.

3. The method of claim 1, further comprising:

associating a speculative bit with said checkpoint and a cache block in said second level circuit, wherein said speculative bit indicates if said cache block is speculative or committed.

4. The method of claim 1, further comprising:

associating a valid bit with said checkpoint and a cache block in said second level circuit, wherein said valid bit indicates if said cache block is valid or invalid.

5. The method of claim 3, further comprising:

associating a valid bit with said checkpoint and a cache block in said second level circuit, wherein said valid bit indicates if said cache block is valid or invalid.

6. The method of claim 5, further comprising:

squashing said stores associated with said checkpoint in said second level circuit by clearing said valid bit, wherein said valid bit is valid.

7. The method of claim 5, further comprising:

committing one or more stores associated with said checkpoint by clearing said speculative and valid bits in said cache block associated with said checkpoint.

8. The method of claim 5, further comprising:

accessing said cache block to interpret said speculative and valid bits for speculative and/or valid states;

associating one or more of said speculative and valid bits with a cache block; and

tracking changes to said one or more of said speculative and valid bits in said cache block.

9. The method of claim 8, further comprising:

moving said store from said cache block to provide space for said subsequent store, when said subsequent store is addressed to said cache block.

10. The method of claim 8, further comprising:

allocating a subsequent cache block when said subsequent store is not addressed to said cache block;

writing said subsequent store to said subsequent cache block; and

updating said one or more of said first and second bits associated with said subsequent cache block.

11. An apparatus, comprising:

a first level store queue adapted to store in an n-entry buffer the last n stores in an instruction window; and

a second level circuit adapted to receive and store non-retired stores from said first level store queue, wherein said second level circuit includes at least one block associated with a checkpoint.

12. The apparatus of claim 11, wherein said second level circuit further comprises:

an address matching circuit; and

a store select circuit, wherein both of said address matching circuit and said store select circuit are adapted to forward stores and store data to any dependent loads.

13. The apparatus of claim 11, wherein said n-entry buffer is a circular buffer with head and tail pointers.

14. The apparatus of claim 11, wherein said second level circuit further comprises:

a memory dependence predictor adapted to store in a non-tagged array one or more store-distances, wherein said store-distance includes the number of store queue entries between a load and a forwarding store.

15. The apparatus of claim 11, wherein said second level circuit further comprises:

an unresolved address buffer adapted to determine a program order condition, wherein said program order condition includes if one or more non-issued load instructions are scheduled ahead of one or more associated store instructions.

16. The apparatus of claim 11, wherein said second level circuit comprises:

a speculative data cache.

17. A system, comprising:

a processor including a first level store queue adapted to store in an n-entry buffer the last n stores in an instruction window, and a second level circuit adapted to receive and store non-retired stores from said first level store queue, wherein said second level circuit includes at least one block associated with a checkpoint;

an interface to couple said processor to input-output devices; and

a data storage coupled to said interface to receive code from said processor.

18. The system of claim 17, wherein said second level circuit further comprises:

an address matching circuit; and

a store select circuit, wherein both of said address matching circuit and said store select circuit are adapted to forward stores and store data to any dependent loads.

19. The system of claim 17, wherein said n-entry buffer is a circular buffer with head and tail pointers.

20. The system of claim 17, wherein said second level circuit further comprises:

a memory dependence predictor adapted to store in a non-tagged array one or more store-distances, wherein said store-distance includes the number of store queue entries between a load and a forwarding store.

21. The system of claim 17, wherein said second level circuit further comprises:

an unresolved address buffer adapted to determine a program order condition, wherein said program order condition includes if one or more non-issued load instructions are scheduled ahead of one or more associated store instructions.

22. The system of claim 17, wherein said second level circuit comprises:

a speculative data cache.